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Box Patent Application
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Washington, DC 20231

Presented for filing is a new provisional-to-utility patent application of:

Applicant: BARMAK MANSOORIAN
Title: HIGH RESOLUTION CMOS CIRCUIT USING A MATCHED IMPEDANCE OUTPUT TRANSMISSION LINE

Enclosed are the following papers, including all those required to receive a filing date under 37 CFR §1.53(b):

	Pages
Specification	9
Claims	4
Abstract	1
Declaration	[To Be Filed At A Later Date]
Drawing(s)	6

Enclosures:

- Postcard.

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Mike Augustine
M.E. Augustine

Under 35 USC §119(e)(1), this application claims the benefit of prior U.S. provisional application 60/093,835, filed July 22, 1998.

This application is entitled to small entity status. A small entity statement will be filed at a later date.

Basic filing fee	$ 0.00
Total claims in excess of 20 times $11.00	0.00
Independent claims in excess of 3 times $41.00	0.00
Multiple dependent claims	0.00
Total filing fee:	$ 0.00

No filing fee is being paid at this time. Please apply any other required fees, **EXCEPT FOR THE FILING FEE**, to deposit account 06-1050, referencing the attorney docket number shown above. A duplicate copy of this transmittal letter is attached.

If this application is found to be INCOMPLETE, or if a telephone conference would otherwise be helpful, please call the undersigned at 619/678-5070.

Kindly acknowledge receipt of this application by returning the enclosed postcard.

Please send all correspondence to:

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Respectfully submitted,

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Enclosures

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: HIGH RESOLUTION CMOS CIRCUIT USING A MATCHED IMPEDANCE OUTPUT TRANSMISSION LINE

APPLICANT: BARMAK MANSOORIAN

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Mike Augustine

M-E Augustine

HIGH RESOLUTION CMOS CIRCUIT

USING A MATCHED IMPEDANCE OUTPUT TRANSMISSION LINE

Cross Reference To Related Applications

This application claims the benefit of the U.S. Provisional Application No. 60/093,835, filed on July 22, 1998.

Background

CMOS active pixel sensor cameras can produce a digital output.

While digital outputs are often relatively noise insensitive, the noise can couple to the analog part of the circuit and cause problems there. Different techniques of minimizing this noise are known in the art.

One way to address the noise is to use current mode transmission of voltages. The current mode transmission can be configured to operate with less noise in certain circuits. However, when current mode transmission is used, other problems can occur. One such problem is a so called ground bounce caused by surges in the power supply.

Summary

The present system teaches a new way of transmitting data from an image chip. This system can increase the signal-

to-noise ratio to thereby increase the rate at which the digital data can be taken off the chip. This enables supporting higher frame rates with high special resolution.

Brief Description of the Drawings

These and other aspects will now be described in detail with the accompanying drawings, wherein:

Figure 1 shows a basic active pixel sensor architecture;

Figure 2 shows a conceptual diagram of current CMOS input/output when viewed as a transmission line;

Figure 3a and 3b show the ground bounce in the CMOS I/O of Figure 2;

Figure 4 shows a new transmission line mode of CMOS I/O;

Figure 5 shows a schematic of a receiver circuit;

Figure 6 shows a first transmitter circuit using all CMOS components;

Figures 7a and 7b show waveforms for the Figure 6 transmitter circuit;

Figure 8 shows a second transmitter circuit using CMOS components and a class A amplifier; and

Figures 9a and 9b show waveforms of the circuit of Figure 8.

Description of the Preferred Embodiment

A disclosed active pixel sensor architecture is shown in Figure 1. This active pixel sensor uses a column parallel approach where an entire column of information is digitized at any one time. More generally, any group of information, where the group could be a column, a partial column, row, partial row or any other group of information, can be simultaneously digitized.

In the architecture shown, the data is digitized at the bottom of each pixel column. The digitized data is then serialized in the internal bus. Data is transmitted through digital output circuitry.

In this disclosed mode, the digitized data is transmitted at 100 megahertz and sent to the imager output pads. This data is then transmitted off the chip.

One bottleneck is caused by the rate at which this digital data can be taken off the imager chip. The design requirements for the I/O circuitry are often more stringent than those in the internal chip. This is because the I/O circuits must be able to drive loads that have large and often unknown parasitic components. The parasitic components can include both capacitive and inductive components. However, the combination of inductive and capacitive parasitics create second order systems that can

have ringing oscillatory behavior at the high transmission frequencies.

The present inventor recognized that the output can be considered as a transmission line. Proper handling of the termination can minimize ringing and oscillatory behavior. The IC 99 shown in Figure 2 is transmitting to a receiving IC 200. A transmission line 210 connects the transmitting IC 99 to the receiving IC 200.

Typical CMOS output circuitry, however, is often not suitable for this transmission line environment. Figure 2 shows the situation of an unterminated CMOS transmission line. Figure 3A and 3B shows respectively the output waveforms when driving coax cable and the glitch voltage at the transmitter ground line. Figure 3A shows the transmission sequence at the output of an unterminated CMOS line. In this system, a voltage equal to VDD/2 is launched into the line at the beginning of the transmission. This voltage travels into the unterminated receiver 200, and at that point is doubled and reflected back. A one-foot length of 50 ohm coaxial cable has a flight time of about 5 nanoseconds. This time increases linearly with the physical length of the cable.

This system, while usable, has certain drawbacks. The output bandwidth is limited. Moreover, the transmitter must wait for the duration of the flight time before attempting another

transition. Also note that the output buffer must supply a current during the entire flight time. This can increase the power consumption of the CMOS output.

Figure 3b shows the voltage in the receiving IC 200. The ground level bounces to add a few hundred millivolts. This can add significant noise onto the voltage output.

Further complication is caused by the characteristic of CMOS that draws current only during the output voltage transitions. Because of the switching variation, there are large variations in current. These variations in current can cause ground bounce and can cause voltage glitches v on the line, of magnitude $V = L\, di/dt$ where L is the inductance of the signal and/or ground bounce. Figure 3b shows these glitches in a single output buffer during a transition. While this diagram is only exemplary, it illustrates the general proposition that a unterminated transmission line will include a reflection, and that the switching techniques of CMOS can also cause ground bounce in this way.

When several buffers switch in tandem, as often happens during digital transmission where multiple bits change state at once, the glitch energies could add. This noise in the power supply line can couple into the analog circuitry in the imager, and can corrupt the pixel outputs.

The problem is addressed by circuit of Figure 4 which shows a current mode signaling system. The voltage swing at the output of a current mode driver can be low or zero, e.g. less than 0.5 volts. This allows the receiver end of the line to be terminated without a large increase in power consumption.

The circuit of Figure 4 can also use a differential mode output. In this situation, the current drawn from the supply is constant. This minimizes glitches on the VDD and on the ground line.

The transmitting IC 400 in Figure 4 drives its transmission line in the form of signal current. The receiver includes, as shown, two common source CMOS transistor pairs, each including an n transistor 410 and p-type transistor 412. The CMOS pair receives the signals at its common source terminal. The drain of the PMOS transistor 412 is biased with a constant current and the output is defined by the drain of the second NMOS transistor. The input impedance for this receiver is defined as the parallel impedance seen at the sources of the n and p channel transistors.

The impedance can be set by adjusting the bias current through the transistors via the current source 420. Once set, the impedance becomes relatively independent of the input current through the configuration. Since the impedance is relatively constant, the reflected signal is minimized and hence transmission speed can be increased.

A more detailed schematic of the receiver circuit 410 is shown in Figure 5. Common source transistors 500, 502 receive the signal at their connected source terminals. The current signal is then mirrored in mirror transistor 504, to form a conventional CMOS logic level. The input impedance for this circuit is set by bias current through current source 508. In this embodiment, the bias current is sent to 3 ma, although the bias current can be changed for different applications.

The circuit 410 shows a dual-ended differential input, with one part on line 503, and the other part on line 501 driving common source transistors 504, 506. Each of the current mirrors 510, 512 change the current to a conventional CMOS level. The circuit can also be used in a single ended mode, by sending only a single line of information.

The output drivers can operate in a current mode output driver mode. Figure 6 shows a first embodiment using a differential pair 600, 602 with open drains that form the differential output. The output impedance of the receiver serves as the load for this circuit. The circuit steers a current that is determined by the bias current source 604 for full differential operation. The logic low level corresponds to negative I bias, and logic high level corresponds to no current.

Figure 7A shows the output waveform of the circuit when driving a 50 ohm, 1 foot coax cable. Figure 7B shows the ground

glitches which are much less than in the previous circuit. The input CMOS voltage 610 is first connected to two CMOS transistor pairs 612, 614. The output of the first stage 612 is buffered by a follower 616, and input to one gate of transistor 602 of the differential pair 600/602.

The voltage V_{IN} is again inverted by the second CMOS transistor pair 614 and input to a second follower 618. Hence, this first current design includes CMOS transistors to buffer and invert the signal as well as two differential followers arranged in a push-pull arrangement, driving a differential pair.

The second embodiment, shown in Figure 8, connects the input CMOS circuit current 604 through a single class A amplifier 800. Again, the input voltage is buffered by first CMOS transistor pair 802, and a second CMOS transistor pair 804 to form both an inverted and a non-inverted signal. These signals are connected to PMOS transistors 806 which are connected to current mirror 808. The output of the current mirror 808 drives the base of a class A transistor 810 which is itself current mirrored by transistor 812. The current mirroring by 812 drives a PMOS transistor 814 that produces the output voltage. A corresponding negative operation to the above produces the negative output voltage 818.

Figure 9A shows a exemplary output, and Figure 9B shows the exemplary ground bounce of such a circuit.

This second embodiment has the additional advantage that is produces a CMOS compatible output voltage when connected to a CMOS IC with high gate impedance.

	Power Consumption mWatts	Ground Bounce mVolts	Bidirectional Operation
Conventional CMOS	33	600	No
Current Mode Design I	10	200	Yes
Current Mode Design II	21	100	Yes

Although only a few embodiments have been described in detail above, other embodiments are contemplated by the inventor and are intended to be encompassed within the following claims. In addition, other modifications are contemplated and are also intended to be covered.

What is claimed is:

1. An image sensor, comprising:

an image acquisition portion;

an image processing portion, receiving image information from said image acquisition portion, said image processing portion including a CMOS circuitry with CMOS outputs having an output impedance; and

an image receiving portion, having an input impedance, receiving said image information from said CMOS outputs, said image processing portion producing a current mode output and said image receiving portion receiving said current mode output; and

an impedance matching device, matching said output impedance of said image processing portion to said input impedance of said image receiving portion.

2. A sensor as in claim 1 wherein said image processing portion includes a portion with a CMOS output.

3. A sensor as in claim 1 wherein said impedance matching circuit comprises a circuit on said image processing circuit.

4. A sensor as in claim 3 wherein an output circuit of said image processing circuit includes a current biased transistor, wherein a magnitude of the current bias sets the output impedance.

5. A sensor as in claim 4 wherein said output impedance is matched to an input impedance of the image receiving circuit.

6. A sensor as in claim 1 wherein said impedance matching circuit comprises a circuit on said image receiving circuit.

7. A sensor as in claim 6 wherein an input circuit of said image receiving circuit includes a current biased transistor, wherein a magnitude of the current bias sets the input impedance.

8. A sensor as in claim 4 wherein said input impedance is matched to an output impedance of the image processing portion.

9. A sensor as in claim 1 wherein said impedance matching circuit comprises a first circuit on said image processing circuit and a second circuit on said image receiving circuit.

10. A sensor as in claim 9 wherein said first and second circuits include current biased elements, and wherein a magnitude of the current bias sets the output impedance.

11. A sensor as in claim 4 wherein said output impedance of said image processing circuit is matched to an input impedance of the image receiving circuit.

12. A sensor as in claim 1, wherein said image receiving circuit includes a current mirror part, that mirrors an input current.

13. A sensor as in claim 1 wherein said image acquisition circuit is an active pixel sensor with a photosensor, an in-pixel buffer, and an in pixel select transistor.

14. A sensor as in claim 13 wherein said an image acquisition portion and said image processing portion operates at substantially zero voltage.

15. An image sensor, comprising:

an image acquisition portion;

an image processing portion, receiving image information from said image acquisition portion; and

an impedance matching device, matching said output impedance of said image processing portion to said input impedance of said image receiving portion by adjusting bias current through at least one biased device in a way that renders the impedance relatively independent of input current.

16. An image sensor as in claim 15, wherein said image acquisition portion and said image processing portion each operate in current mode.

17. An image sensor as in claim 16, wherein said portions operate at substantially zero voltage.

HIGH RESOLUTION CMOS CIRCUIT

USING A MATCHED IMPEDANCE OUTPUT TRANSMISSION LINE

Abstract

Image sensor with CMOS output, an another circuit receiving input. The circuit operates like a transmission line, in current mode, with substantially zero voltage. The impedances are matched by setting bias currents.

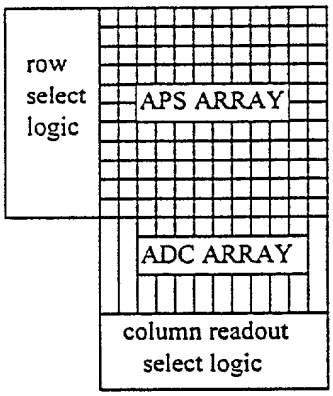

Figure 1 column parallel architecture for focal plane A/D conversion

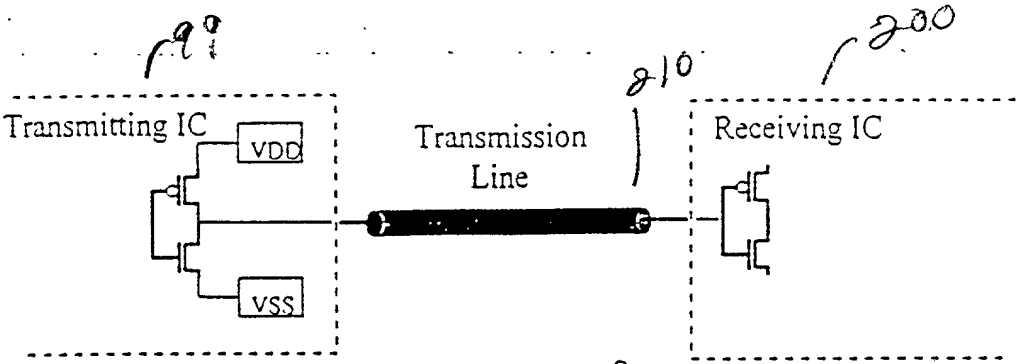

FIG 2

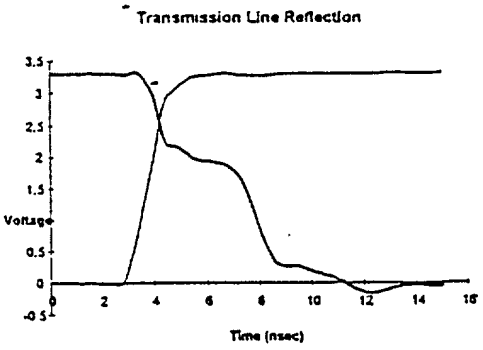

FIG 3a

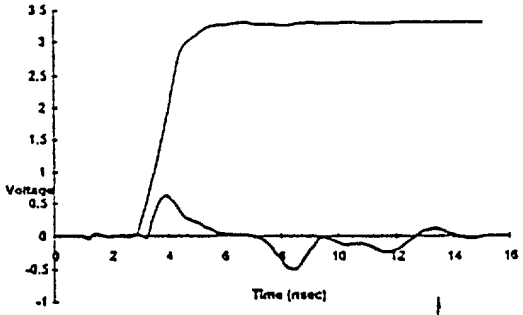

FIG 3b

Figure 1 (a) Conceptual diagram of standard CMOS I/O. (b) Output waveform when driving 1ft of coax cable. (c) Glitch voltage at the transmitter ground line.

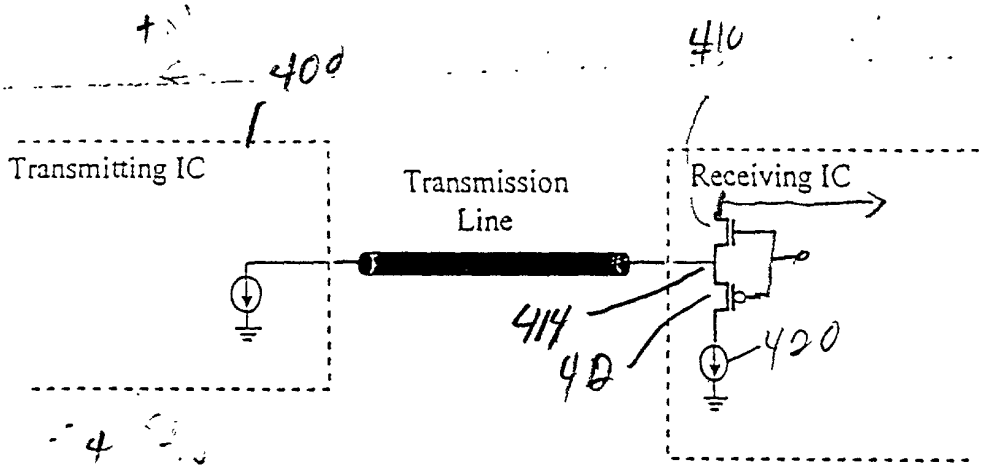

Figure 1 Conceptual sketch of CMOS current mode I/O technique

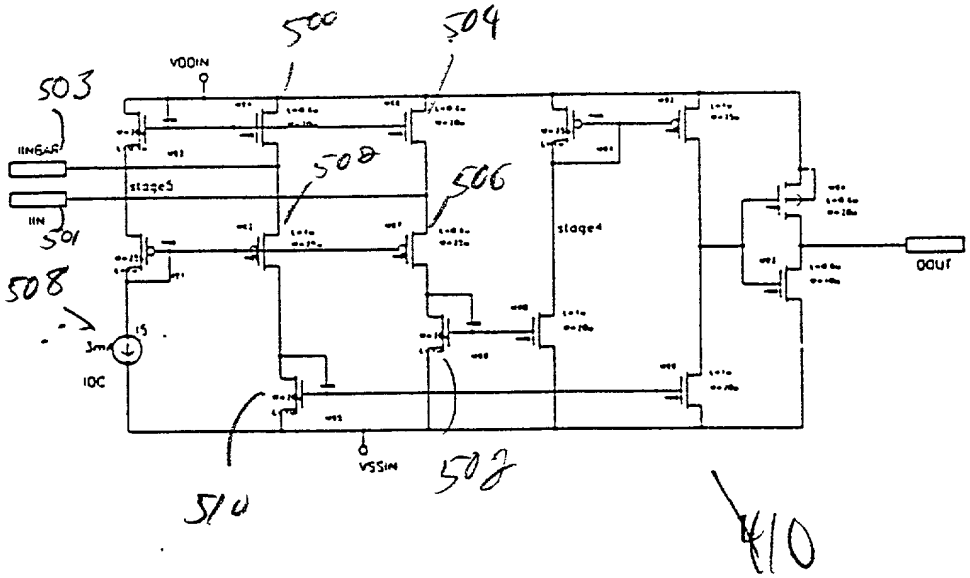

Figure 5 Schematic of receiver circuit.

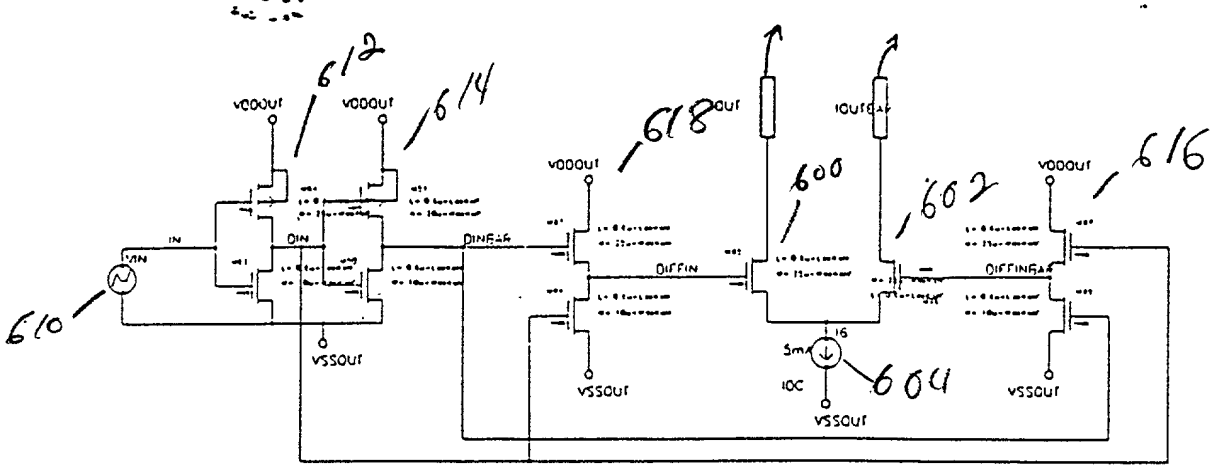

FIG 6

(a)

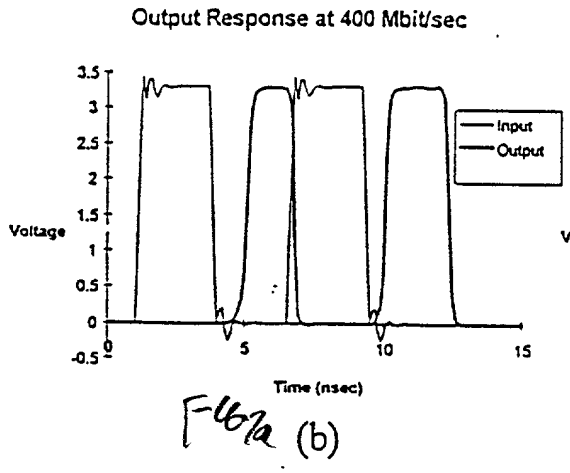

FIG 7a (b)

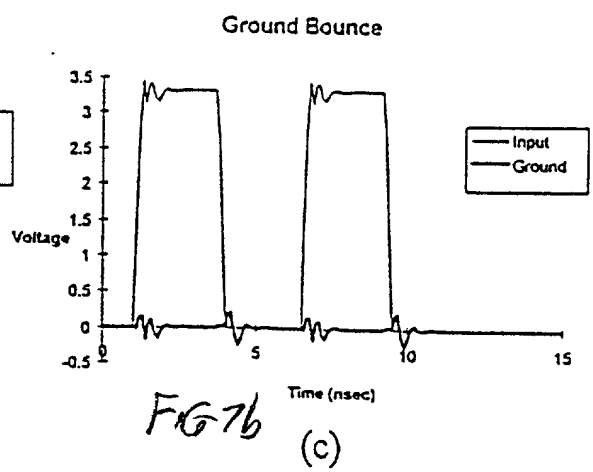

FIG 7b (c)

Figure 1(a) Schematic diagram of 1st output buffer. (b) Output waveform. (c) Glitch voltage at the ground line.

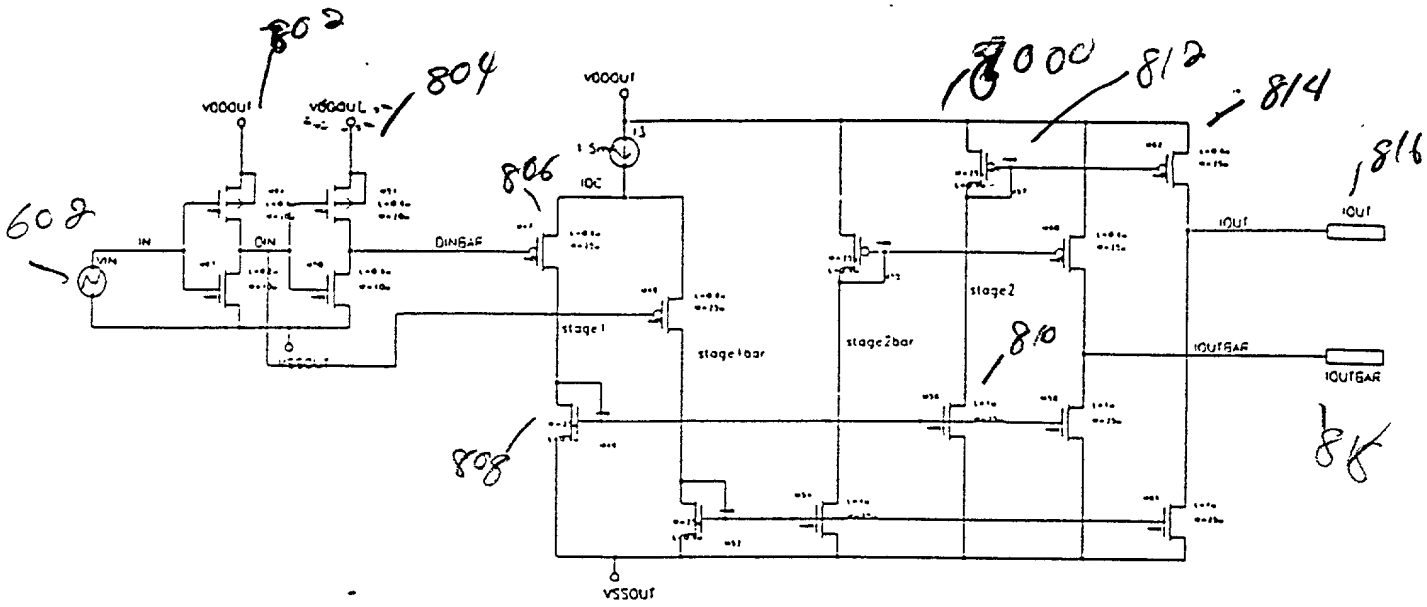

FIG 8

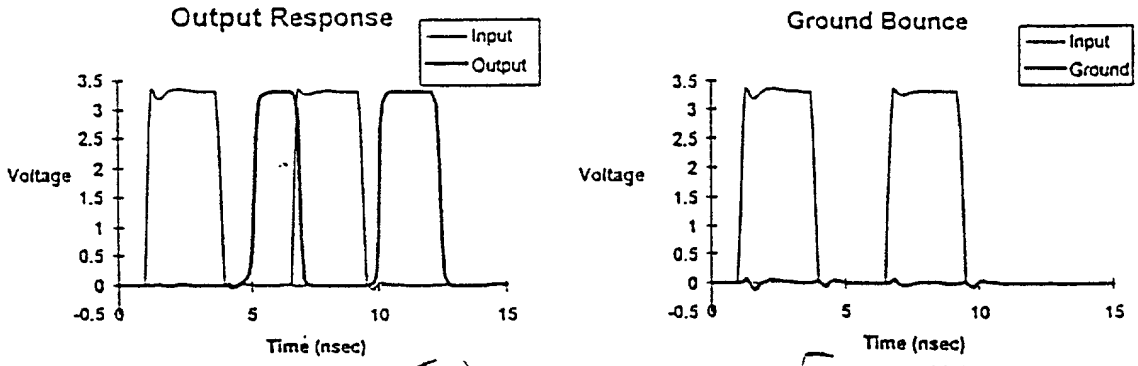

FIG 9(a) FIG 9(b)

Figure 8(a) Schematic diagram of 2nd output buffer. (b) Output waveform. (c) Glitch voltage at the ground line.